



BESS Self-Qualification Guidelines v1.0

Application Note

Document History

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BESS Self-Qualification Guidelines

This guide defines the partner-run qualification process for BESS systems that support AI load buffering, demand response (DR), and low voltage ride-through (LVRT) in grid-connected and islanded onsite generation modes. It explains the required scope, evidence, and submission-ready outputs partners must provide for NVIDIA review.

What Is BESS?

A Battery Energy Storage System (BESS) is a grid-interactive power asset that combines battery modules, bidirectional power conversion systems (PCS), controls, and protection functions to store electrical energy and dispatch active/reactive power in response to grid and load conditions.

Qualification Objective

This qualification includes the following objectives:

- Verify availability and performance of a grid-adaptive, PCS-based BESS.
- Validate dynamic real/reactive response, current limiting, ride-through, islanded stability, black start, and seamless grid-island transitions.
- Provide telemetry and control-transparency evidence sufficient for technical review.

Qualification Workflow

1. Confirm qualification scope and boundary conditions on this page.
2. Run all required tests in [Qualification Tests](#).
3. Prepare your packet using [Submission Procedure](#) and [Appendix A-D: Submission & Standards](#).
4. Complete quality evidence in [Quality and Reliability](#) before submission.

Submission Expectation

Once testing is complete, submit all data to NVIDIA for review and approval. Submissions must include all information necessary to demonstrate compliance with each requirement. Any requirement changes must be reviewed and approved by the owner representatives.

**Note: Qualification Boundary**

This self-qualification explicitly defines the BESS boundary at the AC terminals (PCS inclusive) because the BESS is being qualified as a grid asset. The qualification addresses PCS performance behavior—a gap no existing standard fills. Site transformers, line reactors, switchgear, relays, generators, and campus control systems are outside the scope of this qualification. However, the partner must provide models and evidence sufficient for NVIDIA to validate site-level integration.

**Note: Important**

Passing qualification does not imply site-level stability. However, failure to demonstrate stability across the defined SCR, impedance, and load envelopes constitutes BESS non-qualification regardless of downstream integration.

Qualification Boundary — Excluded Domains

The following domains are deliberately excluded from this qualification scope because they fall under OEM responsibility or existing regulatory frameworks.

Battery Sizing

Battery sizing is irrelevant to qualification. Test 11 (SOC Drift) requires control logic to manage energy balance. Oversizing the battery does not satisfy this requirement. Any reasonably sized system with well-tuned controls should be able to pass.

DC Blocks

DC block topology is outside the qualification boundary, which is defined at the AC terminals. Vendors may use a single large DC block or multiple smaller blocks but must demonstrate compliance at the point of interconnection (POI).

Cell Chemistry

Cell chemistry affects energy density, cycle life, and cost, all of which are OEM decisions beyond this qualification's scope. The tests (ramp response, current limit, LVRT) are chemistry-agnostic by design. A system passes or fails based on PCS behavior alone.

Cybersecurity

Cybersecurity requirements for grid-interactive devices, including BESS PCS, are governed by existing frameworks such as NERC CIP, IEC 62443, and NIST CSF. These standards bodies and regulatory bodies already own this domain. NVIDIA applies those requirements broadly to all IoT devices, including BESS PCS, rather than introducing a redundant or potentially inconsistent parallel requirement.

Safety

Safety requirements, including fire suppression, NFPA 855, UL 9540A, seismic, and related standards, are governed by the Authority Having Jurisdiction (AHJ) and applicable regulatory bodies, not by NVIDIA. NVIDIA is not a safety certification body, and duplicating those requirements here would be redundant and outside the scope of this qualification.

Use Cases for BESS

The BESS qualification addresses the following primary use cases for grid-interactive battery energy storage at AI data center campuses:

- **Low Voltage Ride-Through (LVRT)** — Maintain continuous operation during grid voltage disturbances, preventing costly IT load interruptions.
- **Dynamic AI Transient Reduction** — Buffer rapid power ramps generated by AI workloads to prevent source instability and POI violations.
- **Demand Response (DR)** — Dispatch stored energy on command to reduce peak grid draw while preserving buffering and ride-through reserves.
- **Source Transfer** — Enable seamless transitions between grid-connected and islanded operating modes without loss of load.
- **Black Start** — Energize a de-energized bus and establish stable voltage and frequency to restore site power independently.

General Expectations

Partners must follow this guideline exactly. Submissions must be clear, complete, and technically defensible.

Minimum Expectations

- All acronyms defined on first use
- All tests include raw time-series data at required sampling rates
- All plots include axis units, ranges, and timestamps
- Any deviation from requirements requires a written deviation request and proposed mitigation
- Partners must provide both:
 - Hardware test evidence (bench, HIL, factory test, or field test), and
 - Model evidence (EMT modeling + small-signal) for untestable edge cases
- Submissions must include all information necessary and sufficient to demonstrate compliance

**Warning: No Marketing Claims Accepted**

If a capability is claimed, it must be demonstrated with data and/or validated models.

Confidentiality

All materials provided under this qualification process are treated as NVIDIA Confidential and subject to applicable non-disclosure agreements.

- Partners may designate proprietary implementation details (e.g., controller source code, internal firmware) as restricted
- Measured performance data, test results, and qualification outcomes are not considered proprietary
- Encrypted or compiled models are acceptable, provided they are runnable and allow modification of external grid and load parameters

- Claims of confidentiality may not be used to withhold data required to verify compliance

BESS Qualification Overview

Step 1: Product Requirements Document (PRD) Review

Partner must respond to each PRD requirement line with:

- **Compliant / Non-compliant / Exception** (C, D, or E)
- For non-compliance: current behavior, roadmap, workaround, and risk
- For exceptions: explain the technical substitute and results
- Reference to specific evidence: test ID, plot, model, or certificate

Reference document: **“BESS Requirements Document”**

Table 1. BESS Qualification PRD Response Example

Requirement ID	Item	Description	Partner Response
CTRL-REQ-01	Grid-Adaptive	PCS shall sustain stable island mode operation, including voltage and frequency control independent of grid synchronization signals such as a phase-locked loop (PLL).	Compliant. Evidence: Test 9, EMT case E-4
PERF-REQ-02	Ramp limit	Demonstrate active ramp-rate smoothing to buffer the source from sudden AI load swings. The system must maintain constant stability between the source and the load, ensuring no oscillations or control ‘hunting’ occur during rapid power transitions or under normal load conditions.	Compliant. Evidence: Test 4, 5 and 11



Note:

Since the qualification boundary is at BESS AC terminals, “POI ramp” requirements are verified using an approved POI proxy: a commanded P profile equivalent to the required POI shaping, and/or EMT verification using partner-provided models.

Step 2: Materials, Safety, and Compliance Disclosure

Partner must complete disclosure tables for:

2.1 Battery and PCS Materials and Safety

- Cell chemistry, enclosure type, fire detection/suppression approach
- Cooling method (air/liquid), coolant type (if applicable)
- Dielectrics/insulation class for major components
- Hazardous materials declaration (electrolyte class, refrigerants)

2.2 Standards and Regulatory Compliance Evidence

Provide certificates or reports for:

- UL 9540 / UL 9540A (or equivalent) status
- NFPA 855 alignment statement
- IEEE 2800 functional alignment statement (even if not certified)
- CE/UKCA (where applicable)
- RoHS/REACH
- EMC compliance evidence relevant to PCS

Step 3: Core Requirements Availability

A subset of requirements is designated Core Requirements representing minimum essential capabilities to pass qualification. Partners must complete the “Core Requirements Checklist” provided in [Appendix B](#).

Table 2. Core Requirements (Minimum)

No.	Core Requirement	Requirement ID	Minimum Requirement
1	Autonomous Island Operation Capability	CTRL-CORE-01	PCS shall stably transition to and sustain island mode operation. Loss of external voltage reference shall not cause voltage and frequency regulation to exceed specified performance limits. Voltage source behavior under current limit. Defined virtual impedance or equivalent mechanism.
2	AI buffering dynamic response	PERF-CORE-01	Demonstrate active ramp-rate smoothing to buffer the source from sudden AI load swings. The system must maintain constant stability between the source and the load, ensuring no oscillations or control

No.	Core Requirement	Requirement ID	Minimum Requirement
			'hunting' occur during rapid power transitions or under normal load conditions.
3	Current limit behavior	PERF-CORE-02	Current limiting shall be predictable: no unstable oscillation, no uncontrolled voltage collapse in modeled grid conditions.
4	LVRT/HVRT	GRID-CORE-01	Support IEEE 2800 ride-through behavior as baseline; utility curves may supersede.
5	Reactive power support	GRID-CORE-02	Provide voltage support via Q within PCS current limits; document Q priority rules.
6	Seamless grid/island transition	MODE-CORE-01	Demonstrate controlled transitions without loss of synchronism or unstable control mode hunting. Transition performance shall be quantified using voltage deviation per ANSI C84.1 and dynamic voltage/frequency ride-through per IEEE 2800.
7	Black start	MODE-CORE-02	Demonstrate black-start energization of a dead bus and stable V/f regulation.
8	Telemetry and controls	TELE-CORE-01	Real-time reporting of V, I, P, Q, f, SOC, alarms, and limit states. Must support 3 concurrent Modbus TCP connections with all points being polled at 1 second frequency. SOC values must be included in all telemetry reporting.
9	Control transparency artifacts	MODEL-CORE-01	Provide EMT model + validation against impedance/admittance scan (dq impedance vs frequency) + Nyquist/passivity artifacts. Comply with NERC Reliability Guidelines.
10	DR dispatch capability	OPS-CORE-01	Follow dispatch setpoints with defined response time, ramp limits, and SOC reserve logic.

Step 4: Qualification Tests

This section defines test procedures and pass/fail criteria. All tests are performed at the BESS AC terminals unless explicitly stated as model-only.

Table 3. Instrumentation Requirements (applies to all tests)

Minimum measurement accuracy (applies to all tests):

Parameter	Minimum Accuracy	Sampling Rate
Voltage	±0.2% of reading	≥ 5 kHz (EMT) / ≥ 10 Hz (operational)
Current	±0.2%	≥ 5 kHz (EMT) / ≥ 10 Hz (operational)
Power (P/Q)	±0.5%	≥ 10 Hz
Frequency	±0.01 Hz	≥ 10 Hz
Time Sync	±1 ms between channels	N/A

Parameter	Minimum Accuracy	Sampling Rate
P/Q Dynamic (ramp, oscillations and transients)	$\pm 0.1\%$ of rated P at test frequency	≥ 120 Hz
Bandwidth	0.1–59.9 Hz	—

All events must include pre-trigger (≥ 5 s) and post-trigger (≥ 20 s) unless otherwise specified.

Qualification Tests

Test 1: Telemetry Verification and Data Integrity

Objective: Verify PCS telemetry accuracy, timestamping, and completeness.

Steps

- Operate PCS at 10%, 50%, 75% and 100% rated MW in grid-connected mode
- Record internal telemetry and compare to external 0.5S (IEC 62053-22) or better revenue-grade meters
- Verify by demonstration reporting of: V, I, P, Q, f, SOC, PCS temperature, current limit flags, mode state
- Event logging shall be 1 ms precision
- Logs shall be held for 7 days minimum
- Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above

Pass Criteria

- > P and Q error $\leq \pm 0.5\%$ or better of reading across points
- > Time alignment error ≤ 5 ms
- > No missing channels, no “flatlined” sensors

Test 2: Grid-Adaptive Voltage and Frequency Regulation (Islanded)

Objective: Demonstrate stable operation with no external grid reference.

Setup: Isolated test bus with configurable resistive/inductance/capacitance (RLC) load bank.

Steps

- Black start onto dead bus (if Test 10 not yet done, run reduced voltage)

- Hold voltage and frequency within the system's defined stability limits at a steady load
- Apply load steps: +10%, +20%, -20% of PCS rated MW
- Record V, I, P, Q, f, and control mode state throughout the test
- Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria

- > Stable V/f with no sustained oscillation
- > Voltage and frequency return to their steady-state range in a timely, well-damped manner, with no evidence of control hunting or marginal stability
- > No protective trip

Test 3: Current Limit Characterization (P-first, Q-first, and Mixed Priority)

Objective: Demonstrate stable, predictable, and transparent PCS behavior when operating at or beyond current limits under all priority configurations.

Steps

- Force the PCS into current limit using:
 - Reduced-voltage condition on the test bus
 - Commanded P and/or Q beyond the declared capability envelope
- Repeat for each priority configuration:
 - Active power (P) priority
 - Reactive power (Q) priority
 - Partner default or "grid-support" mode
- Record P, Q, V, I, current-limit flags, and control-mode state variables
- Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria

- > PCS remains stable and controllable while in current limit
- > PCS explicitly reports entry into and exit from current limit via telemetry
- > Control priority and available headroom are observable and consistent with documented behavior

Disqualification Criteria

- > **Limit-cycle oscillation:** Under steady-state operating conditions, no sustained oscillations shall be present, and PCS performance shall remain within all applicable generator and grid interconnection requirements.
- > **Control-mode hunting:** More than one control-mode transition (e.g., P→Q→P, GFM→GFL, or equivalent) during a single current-limit event constitutes test failure.
- > **Voltage recovery behavior:** Upon release from current limit, terminal voltage shall recover monotonically to its regulated setpoint. Any overshoot, undershoot, or oscillatory recovery exceeding $\pm 5\%$ of nominal voltage constitutes test failure.

Deliverables

- Demonstrate through EMT analysis
- P–Q capability map with clearly defined current-limit envelope
- Annotated time-series plots showing:
 - Entry into current limit
 - Behavior while limited
 - Exit from current limit and voltage recovery
- Description of current-limit implementation and priority logic

Test 4: AI Buffering Proxy Test (Fast Ramp Tracking)

Objective: Demonstrate the BESS can buffer AI-induced power ramps at the required rate without inducing control instability.

Steps

- Operate PCS in grid-connected mode at both weak-grid ($SCR \leq 3$) and strong-grid ($SCR \geq 20$) configurations
- Apply a time-varying active power command profile that is representative of realistic AI workload ramps, including both short bursts and longer ramp intervals, and reaching ramp rates up to the vendor's declared AI-buffering capability. Partner must state the assumed IT load used for the test and demonstrate correct scaling of results.
- Record P, Q, V, I, and current-limit and control-mode state flags
- Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above.

Pass Criteria

- > **Tracking accuracy:** Steady-state ramp tracking error $\leq 2\%$ of commanded ramp magnitude
- > **Current limit:** No entry into current limit during execution of required buffering profile
- > **Stability:** No sustained oscillatory behavior induced by control interaction

Disqualification Criteria

- > **Sustained oscillation:** Any clearly observable, sustained oscillatory behavior in measured P, Q, V, I, or frequency that indicates marginal or unstable control response during the ramp profile constitutes test failure, regardless of steady-state tracking accuracy.
- > **Current-limit interaction:** Repeated or sustained entry into current limit, as indicated by PCS telemetry or limit-state flags, during execution of the required buffering profile constitutes test failure, unless explicitly declared as outside the partner's stated capability envelope.
- > **Ringling tolerance:** Short-duration transient ringing (less than one second) is acceptable only if it is monotonically decaying, does not re-enter current limit, and does not induce control-mode transitions.



Note:

This test does not, by itself, prove site POI compliance. It verifies that the PCS can execute the required buffering action when properly integrated.

Test 5: AI Buffering EMT Validation (Model-Based, Required)

Objective: Validate PCS stability and control robustness under extreme weak-grid conditions representative of faulted, partially islanded, or switching-dominated AI campus scenarios.

Partner Provides

- EMT model of PCS + controls (compiled or encrypted acceptable, but must run)
- dq impedance curves vs frequency
- Nyquist or passivity evidence

Required EMT Case

- **SCR:** 2.0
- **Grid impedance:** Sweep from X/R ratio = 2 to 10, representative of inverter-dominated grids
- **Topology:** Grid-connected with upstream source modeled as weak voltage source

- **Load:** Constant Power Load representative of IT/compute with clearly defined ramp characteristics shall be used

Disturbances to Apply

- AI buffering proxy ramps
- At least one grid disturbance event (voltage dip, impedance step, or partial islanding)
- Entry into and recovery from PCS current limit

Steps

- Configure the EMT model with the required case parameters above
- Apply each disturbance scenario sequentially, recording all state variables
- Provide all model outputs and analysis necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above

Pass Criteria

- > POI ramp compliance for the defined workload profile
- > No unstable oscillation modes across operating range
- > System remains stable with no loss of synchronism
- > No sustained oscillatory modes
- > No uncontrolled voltage collapse at the BESS terminals
- > PCS transitions into and out of current limit in a controlled and documented manner

Failure Criteria

- > Any unstable oscillation persisting more than one second
- > Voltage collapse or failure to recover to regulated operating point
- > Control mode hunting or undefined control state transitions
- > Model instability that prevents completion of the test scenario



Note:

This stress case may be performed model-only.



Warning:

Failure in this case constitutes non-qualification, regardless of performance at higher SCR values. This test is intended to expose control fragility under realistic worst-case grid conditions expected in large AI campus deployments.

Test 6: Demand Response Dispatch Performance

Objective: Verify DR execution without breaking buffering and ride-through reserves.

Steps

- Demonstrate dispatch steps at: 10%, 25%, 50%, 100% of DR committed MW
- Demonstrate ramp-limited dispatch (partner must implement ramp limits)
- Demonstrate SOC reserve policy: hold back prescribed SOC capacity reserved for LVRT/buffering
- Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above

Pass Criteria

- > Commanded MW achieved within specified response time (default: 2 s for fast DR, 60 s for slow DR)
- > No violation of SOC reserve rules
- > Clear state machine behavior when DR conflicts with LVRT

Deliverable: DR state machine diagram and priority rules

Test 7: LVRT / HVRT Functional Ride-Through (Hardware or HIL)

Objective: Prove ride-through behavior aligned to IEEE 2800 baseline.

Steps

- Apply voltage sag and swell profiles at AC terminals (grid simulator or HIL) at both weak-grid ($SCR \leq 3$) and strong-grid ($SCR \geq 20$) configurations:
 - Multiple depth-duration points per IEEE 2800 or utility categories
- Observe whether PCS stays connected and how it prioritizes Q support
- Record V, I, P, Q, f, and protection relay states throughout each ride-through event
- Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above

Pass Criteria

- > No trip within IEEE envelope or applicable utility/ISO envelope, whichever governs
- > Correct trip outside envelope
- > Q injection behavior documented and consistent

Test 8: Seamless Grid / Island Transition

Objective: Validate transition logic and stability.

Steps

- Start grid-connected in buffering mode
- Execute intentional islanding event (open upstream breaker) while load present
- Maintain V/f and continue supplying load
- Resynchronize and reconnect to grid with controlled closing logic
- Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above

Pass Criteria

- > No unstable mode hunting
- > No uncontrolled frequency drift
- > Reclose without excessive inrush or protective trips
- > Event logs show proper sequencing

Test 9: Islanded Operation with Generator Following (Model-Based)

Objective: Validate interaction with turbines or gensets.

Steps

- EMT model with GFM BESS as voltage master
- Generator modeled as droop-following source with realistic governor time constants
- Apply AI load proxy disturbance and show:
 - BESS absorbs fast dynamics

- Generator picks up slower energy component
- Include N-1 generation event
- Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above

Pass Criteria

- >
- > No sustained oscillation
- > SOC drift controlled (see Test 11)
- > Frequency and voltage remain within declared bounds

Test 10: Black Start

Objective: Demonstrate ability to energize a dead bus and establish stable V/f.

Steps

- PCS starts from de-energized condition
- Energize test bus to nominal voltage
- Pick up load in steps: 10%, 25%, 50% rated
- If using auxiliary supply, document requirements
- Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above

Pass Criteria

- > Stable energization
- > No nuisance trips
- > V/f regulation within declared bounds

Test 11: SOC Drift and Energy Management Under Combined Missions

Objective: Demonstrate that the BESS can simultaneously support AI buffering, demand response, and LVRT reserve obligations over time without uncontrolled state-of-charge (SOC) drift.

Test duration: Minimum 24-hour continuous simulation or accelerated profile test.

Steps

- Run a 24-hour simulation or accelerated profile test:
 - AI buffering proxy ramps applied intermittently throughout the test window
 - Demand response dispatch events of varying magnitude and duration
 - At least one LVRT or equivalent grid-disturbance event
 - Declared SOC operating window and reserve thresholds enforced
- Provide all test data necessary and sufficient to demonstrate compliance with the requirements and pass/fail criteria above

Pass Criteria

- > **Net SOC drift:** $\leq \pm 5\%$ of usable SOC capacity, excluding declared DR events
- > **SOC bounds:** Remain within partner-declared operating window at all times
- > **Energy prioritization:** Explicit de-prioritization when approaching reserve thresholds

Disqualification Criteria

- > **Unbounded SOC drift:** Exceeding $\pm 5\%$ without declared external energy imbalance
- > **Undefined reserve behavior:** Loss of capability without explicit state transition
- > **Implicit behavior:** SOC management relying on undocumented heuristics

Required Deliverables

- Time-series plots of SOC, P, Q, service state, and reserve flags
- Energy balance summary table (in/out, losses, DR energy, net drift)
- State machine diagram showing:
 - Normal operation
 - Reserve-threatened operation
 - De-rating or service shedding behavior
- Event log with timestamped state transitions and priority changes



Note: Important

Oversizing battery capacity alone does not satisfy this requirement. SOC stability must be achieved through control logic and energy management, not nameplate capacity.

Test 12: Control Transparency Package Review

Objective: Provide the analysis artifacts needed for integration.

Required Deliverables

- EMT model package with instructions
- dq or sequence (full matrix) impedance vs frequency (magnitude and phase) in key operating points, at least +0.9 p.u. and -0.9 p.u. active power
- Nyquist plot or passivity assessment demonstrating stability margin for extremely weak (SCR = 2, X/R = 10) and strong grid conditions (SCR = 20, X/R = 10)
- Controller description: loops, bandwidths, current limit behavior
- Parameter list: droop coefficients, virtual impedance, inertia, PLL state (if any)

Pass Criteria

- > Package is complete, runnable, and consistent with measured behavior
- > No “black box with no stability evidence” accepted
- > Has snapshot feature to start simulations from a specific snapshot
- > Model runs with generally accepted Fortran compilers released after 2018

Business and Supply Chain Readiness

In addition to technical qualification, partners must demonstrate credible readiness to support AI-scale deployment timelines. This includes proven manufacturing throughput, realistic ramp capability, and supply chain resilience aligned with multi-hundred-MW to GW-scale deployments.

Demonstrated Manufacturing Throughput

Partners must disclose actual, historical production capability, not theoretical capacity.

Required Disclosures

- Annual PCS throughput delivered in the most recent 12-month period (MW/year)
- Largest single PCS or BESS deployment delivered to date (MW and delivery timeframe)
- Current factory locations supporting PCS production and final integration
- Current average and worst-case lead times for PCS delivery

Evidence Required

- Shipment records or customer references
- Factory acceptance test (FAT) throughput data
- Identification of binding constraints (labor, test infrastructure, power electronics, controls)

Scale Ramp Credibility (10× Within 24 Months)

Partners must present a credible, executable plan to scale PCS manufacturing throughput by an order of magnitude (10×) within 24 months.

Required Elements

- Baseline throughput (MW/year) and target throughput (MW/year)
- Time-phased ramp plan with quarterly milestones

- Critical path items: power semiconductor supply, control hardware, test infrastructure, labor
- Capital investments required (facilities, tooling, test equipment)
- Dependencies on single-source or constrained sub-suppliers

Supply Chain Resilience and Risk Disclosure

Required Disclosures

- Single-source components and mitigation plans
- Geographic concentration risks (manufacturing, sub-tiers)
- Long-lead components and committed capacity
- Inventory buffering strategy for critical components
- Exposure to export controls, trade restrictions, or geopolitical risk

Failure Mode Acknowledgment

Partners must explicitly identify scenarios in which scale targets cannot be met.

- Conditions under which throughput ramp would be delayed or capped
- Contingency plans and alternative sourcing strategies
- Clear articulation of commitments under accelerated demand scenarios

Industrial Standards and Regulatory Certificates

Partners must provide a list of industrial standards the system is designed to comply with (e.g., IEEE, IEC, GB), as well as test certificates (e.g., UL, CSA, CE, CCC) granted by countries or economic areas for installation and operation.



Warning: Evaluation Note

Lack of demonstrated historical throughput or absence of a credible scale-up plan constitutes **business non-qualification**, regardless of technical performance. This section is intended to surface manufacturing reality early, not after technical qualification.

Quality and Reliability

This section defines the minimum quality system evidence and reliability substantiation required for BESS qualification. The intent is to prevent “passes on paper” where functional tests succeed but field reliability is unacceptable.

Quality Management System and Traceability

Required Submissions

- **QMS certification:** ISO 9001 certificate (or equivalent), including scope and certified sites
- **Change control process:** Documented ECN/ECO process with revision control
- **Supplier quality:** Supplier qualification process, incoming inspection, SCAR workflow
- **Traceability:** Lot traceability for battery cells, power semiconductors, capacitors, magnetics, control boards
- **Serialization:** Unique serial numbers at rack, PCS, and critical subassembly level
- **Nonconformance system:** NCR process, RCA expectations, and closure criteria
- **CAPA:** Metrics and example packages from the last 12 months

Reliability Targets and Definitions

Minimum Required Declarations

- Availability target for the qualified configuration
- MTBF / MTTF definitions and calculation method
- Failure rate assumptions and confidence bounds
- AFR for major replaceable units (PCS power stage, controller, cooling system, BMS, contactors)

- Mission profile including ambient range, load profile, switching frequency, current-limit time fraction, SOC window



Caution: Critical Requirement

If the partner cannot defend reliability numbers under an AI buffering duty cycle, the system fails qualification regardless of lab functional results.

Reliability Model and Evidence Requirements

- Reliability block diagram (RBD) showing system topology and redundancy
- FMEA/DFMEA and PFMEA with top 20 risk items and mitigations
- Parts stress and thermal analysis for the PCS
- Reliability prediction method and justification
- Field reliability evidence (if product is deployed)

Environmental and Durability Qualification

- Thermal performance and derating curves
- Thermal cycling test results
- Vibration and shock testing (ISTA or IEC 60068 equivalent)
- Ingress protection (IP/NEMA rating evidence)
- Corrosion / contamination robustness
- Acoustic and mechanical resonance risks

Power Electronics Reliability and Protection Robustness

- Protection coordination philosophy inside the PCS
- Short-circuit and fault withstand capability
- Grid disturbance robustness
- Harmonic and ripple limits

Battery System Reliability and Safety Monitoring

- Cell and module qualification basis
- BMS robustness and fault detection coverage
- Thermal management reliability
- Degradation model and capacity fade predictions, including degradation rates based on shallow discharges at a variety of SOC levels
- Maintenance intervals and remote diagnostics capability

Factory Acceptance, Production Testing, and Burn-In

- Factory Acceptance Test (FAT) procedure
- Production test coverage (every unit vs sampling)
- Burn-in or screening for infant mortality
- Calibration and metrology schedule

Serviceability, Spares, and Mean Time to Repair

- MTTR assumptions and basis
- Spare parts list with recommended on-site spares
- Replaceable unit strategy and hot-swap capability
- 24/7 remote support model and escalation process
- Event logging requirements and export format

Reporting Format and Acceptance Criteria

Partners must submit a single Quality and Reliability Package containing:

- QMS certificates and site scope
- Reliability model (RBD + assumptions) and results
- DFMEA/PFMEA top risks and mitigations
- Environmental qualification reports
- FAT and production test summaries
- Field reliability data with failure mode breakdown

- Maintenance plan, MTTR basis, and spares strategy



Warning: Automatic Fail Conditions

- Missing QMS/traceability evidence
- Reliability predictions not tied to a declared mission profile
- Failure to provide DFMEA/PFMEA and top-risk mitigations
- Field data contradicts claims without explanation and corrective plan

Self-Qualification Packet — Submission Procedure

Step-wise administrative procedure for a BESS partner to assemble and submit a self-qualification packet to NVIDIA. This procedure defines the qualification pathways, ordered packet artifact structure, and per-test evidence map covering all twelve qualification tests.

Companion to: BESS Self-Qualification Guidelines

Audience: BESS Partners and NVIDIA Reviewers

Correspondence: Single channel—Partner and NVIDIA

Governing Principle—Single Channel of Correspondence

The BESS Partner (OEM) **owns compliance** and is NVIDIA's sole point of contact. Regardless of who executes the tests, **all correspondence, submissions, and clarifications flow only between the BESS Partner and NVIDIA**. Test labs and third-party experts are subcontracted to the partner and never correspond with NVIDIA directly.

Figure 1. Correspondence Model



Note: Single Channel Rule

No lab-to-NVIDIA correspondence is permitted. Testing and expertise are subcontracted to the BESS Partner.

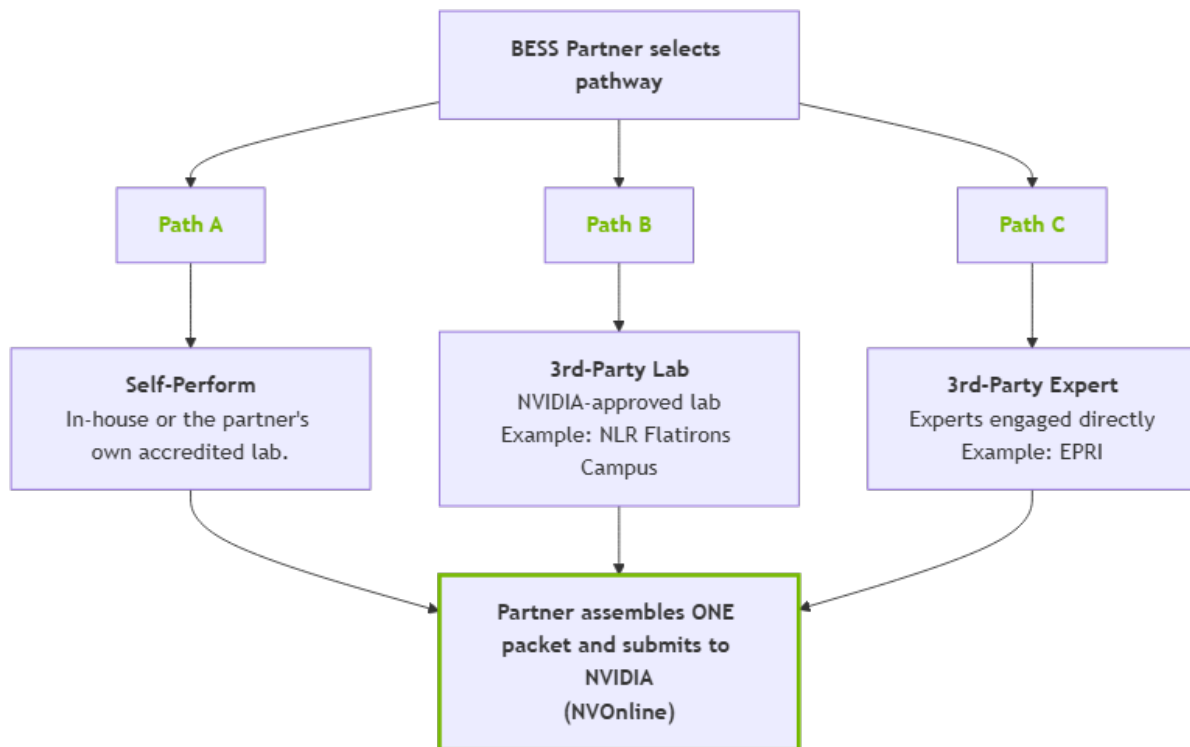
- **NVIDIA Reviewer:** Corresponds only with the BESS Partner.

- **BESS Partner (OEM):** Owns compliance and subcontracts labs/experts as needed.
- **Lab/Experts:** Work for the partner only; no direct lab-to-NVIDIA correspondence.

Qualification Pathways

The partner may choose one pathway for all tests or mix pathways by test.

Figure 2. Pathway Selection



Note: Mixed Pathways Permitted

A partner may mix pathways per test (for example, self-perform Tests 1 to 3, run EMT validation by EPRI, and perform ride-through at Flat Iron). Any third-party work must include signed attestation in Artifact 10.

Step-Wise Administrative Procedure

The following timeline defines the end-to-end administrative workflow, from partner intake through NVIDIA disposition.

Table 4. Process Timeline

Step	Owner	Action	Output
0	Partner	Register & Intake: Register intent, execute NDA, open NVOnline record	Submission record ID
1	Partner	PRD Response: Respond line by line to PRD Table 2 (Core Requirements): Comply / Deviate / Exception	PRD response matrix
2	Partner	Disclosures: Complete materials, safety, and compliance disclosures	Disclosure set
3	Partner	Select Pathway(s): Select pathway A/B/C per test; contract lab/experts if used	Test plan and scope attestation
4	Partner / Lab / Expert	Execute 12 Tests: Execute all twelve qualification tests (hardware, HIL, and model-only as specified)	Raw data and plots per Appendix A
5	Partner	Assemble Packet: Assemble packet in required 00-10 artifact order	Complete self-qualification packet
6	Partner	Submit: Submit package via NVOnline (Appendix E steps)	Submitted packet and notification
7	Partner and NVIDIA	Review & Clarification: Resolve review comments through single channel	Resolved review log
8	NVIDIA	Disposition: Issue disposition: Qualified / Conditional / Gaps	Qualified products may be listed on Marketplace (best effort)

Prescribed Packet Artifact Order

Submit as a single indexed package (folders or a bookmarked PDF) using *exactly* this numbering. Each folder maps to a section of the guidelines so reviewers can navigate directly to governing requirements.

Order	Artifact	Contents / Source
00	Cover sheet and submission letter	Partner, product/model, firmware version, submission ID, pathway(s), single POC
01	Core Requirements Checklist	Appendix B mapping: Core Requirement -> Test IDs -> Evidence reference (reviewer's index)
02	PRD Response Matrix	Product Requirements Doc—line-by-line response to PRD Table 2 Core Requirements: Comply / Deviate / Exception
03	Materials, Safety and Compliance Disclosures	Disclosure tables from Step 2
04	Standards and Regulatory Certificates	Appendix D : IEEE 1547/2800, UL 9540/9540A, NFPA 855, CE/UKCA, IEC 62443, etc.

Order	Artifact	Contents / Source
05	Test Reports 1-12	One subfolder per test (05-01 to 05-12), each containing Appendix A evidence set
06	EMT / Model Package	Appendix C : EMT model, dq impedance plots, Nyquist/passivity artifact, version-controlled parameter export
07	Business and Supply Chain Readiness	Section 4: throughput, 10×/24-month scale plan, supply-chain risk, failure-mode acknowledgment
08	Quality and Reliability	Section 5: QMS/traceability, reliability targets & model, environmental/durability, FAT/burn-in, serviceability
09	Deviations and Known-Issues Log	Consolidated list across all tests (Appendix A requirement)
10	Third-Party Attestation	Signed statement from Lab/Expert (Path B/C): scope, methods, independence. N/A for Path A

Required Contents for Each Test Report (Folder 05-XX)

This report must be presented in the following order.

1. Test configuration (single-line + controller settings + SOC)
2. Raw time-series data (CSV)
3. Summary plots (PDF)
4. Pass/Fail statement tied to criteria
5. Known issues and deviations ([Appendix A](#))

Test Coverage and Location Map

Test	Title	Type	Report Folder
1	Telemetry Verification and Data Integrity	Hardware (grid-connected)	05-01
2	Grid-Adaptive V/f Regulation (Islanded)	Hardware (islanded bus)	05-02
3	Current-Limit Characterization (P-first / Q-first / Mixed)	Hardware	05-03
4	AI Load Buffering / Ramp-Rate Smoothing	Hardware	05-04
5	EMT Validation (weak grid, SCR sweep)	Model-only (Appendix C)	05-05 + 06
6	Demand Response (DR) Dispatch	Hardware	05-06
7	LVRT / HVRT Ride-Through	Hardware	05-07
8	Grid to Island Transition	Hardware	05-08
9	Generator Following	Hardware	05-09
10	Black Start	Hardware	05-10
11	SOC Drift / Energy Balance	Hardware	05-11

Test	Title	Type	Report Folder
12	Control Transparency	Hardware + Model	05-12 + 06

**Caution: Instrumentation Requirements**

Instrumentation minimums (accuracy, sampling rate, and pre/post-trigger windows) from [Step 4](#) of the BESS Qualification Overview section applies to all tests and must be evidenced in each report configuration section (05-XX, item 1).

Appendix A-D: Submission & Standards

Appendix A: Data Submission Requirements

Every test must include:

- Raw time-series (CSV)
- Summary plots (PDF)
- Test configuration (single-line of test setup, controller settings, SOC)
- Pass/fail statement tied to criteria
- Known issues and deviations list

Appendix B: Core Requirements Checklist

Partners must fill out a one-page checklist mapping: **Core Requirement** → **Test IDs** → **Evidence references**.

Appendix C: Partner Model Package Requirements

Minimum:

- EMT model (PSCAD/EMTDC, RTDS, or equivalent), including control blocks
- dq impedance plots at:
 - 10%, 50%, 100% P
 - High and low Q
 - Multiple SCR values
- Nyquist/passivity artifact and interpretation
- Version-controlled parameter export

**Caution: Model Validity**

Models that cannot reproduce hardware behavior within stated tolerances are invalid.

Appendix D: Industrial Standards and Regulatory Certificates

Partners must provide a list of industrial standards the system is designed to comply with, as well as test certificates granted by countries or economic areas. Key standards include:

- IEEE 1547-2018, IEEE 2800
- UL 9540 / UL 9540A
- NFPA 855
- CE/UKCA
- RoHS/REACH
- IEC 60068
- ISO 9001
- NERC Reliability Guidelines
- NERC CIP (Critical Infrastructure Protection)
- IEC 62443 (Industrial Automation and Control Systems Security)
- NIST Cybersecurity Framework (CSF)

Appendix E: DCE BESS Equipment Qualification Process

NVIDIA defines the bar. Independent testing labs verify. OEMs prove compliance directly to their customer. Marketplace listing is recognition of a process completed — not the gate that allows it.

Roles with Qualification vs. Listing

Party	Role in the Process	Key Responsibilities
NVIDIA	Authors the criteria. Hosts the marketplace. Reviews the lab report at the end of the cycle.	Publishes PRD & test procedures; qualifies third-party labs; reviews final compliance package; lists qualified product (best effort).

The following steps outline the process for submitting completed test reports to NVIDIA for listing on its Marketplace website.

Step 1: Login to NVOnline

Navigate to the NVOnline portal. From the top navigation bar, select the appropriate site for your company. Use the Content Library to access reference documents such as platform design guides and related specifications.



Step 2: Navigate to Report a Bug

From the NVOnline homepage, click the “Bug” menu in the top navigation bar and select “Report a Bug” from the dropdown menu.



Step 3: Fill in the Bug Report Form

Complete the “Report a Bug” form.

Common Form Fields

- **Problem Type:** Select “Qualification Review” from the dropdown
- **Severity:** Low
- **Priority:** 3 - Low
- **Divisions:** Select your company site from the dropdown
- **Issue Type:** Select “Qualification-Review-Issue”
- **Product Segment:** Select “Other”
- **Focus Area:** Select “DC Infrastructure” and then “BESS” from the subcategory dropdown

Synopsis Format by Use Case

The Synopsis field (200 characters maximum) must follow one of these formats:

- **Qualification Review:** Facilities Level - <Supplier Company Name> DC Infrastructure BESS Review

Step 4: Enter BESS-Specific Description (Qualification Review)

For Qualification Review submissions, enter the following information in the Description field. Items marked with <attachment> must be uploaded as file attachments:

1. Subject: Facilities Level - <Supplier Company Name> DC Infrastructure BESS Review
2. MPN: <Supplier part number>
3. Revision: <version>
4. SPEC: Supplier SPEC <attachment>
5. 3D CAD: Supplier CAD <attachment>
6. 2D Drawing: Supplier 2D <attachment>
7. Self Validation Report: Supplier performance validation report per BESS Self-Qualification Guidelines <attachment>

Step 5: Add Members, Upload Attachments, and Submit

Before submitting the bug, complete the following:

1. **Add Members:** In the Cc Details section, add all relevant NVIDIA and partner team members who should be notified of this submission.
2. **Upload Attachments:** In the Attachments section, drag and drop or browse to upload all design files referenced in the description (SPEC, 3D CAD, 2D Drawing, Self Validation Report).
3. **Submit:** Once all details are filled in and attachments are uploaded, click the “Submit Bug” button. You may also use “Save as draft” to save your progress before submitting.

HOME
BUG

REPORT A BUG

Issue Type

Issue Details

Product Details

Additional Information

Attachments

*Problem Type
Qualification Review

Severity
Low

Priority
3 - Low

Fix Needed in PROD by
mm/dd/yyyy

*Synopsis

200 characters remaining (200 maximum)

*Description

A^x v A^y v A^z v Paragraph B I U S ☺ 🔗 📷 🎥 📅 “ ”

***** Instructions for PVP / NVIDIA Qualified Submission *****

1. Select the appropriate product segment, issue type. Set Focus area to 'PVP (NVIDIA Qualified)

2. Please attach all logs and results as part of the PVP sheet (*.xism)

*Divisions:

*Products:

*Operating Systems:

+ Projects

+ Cc Details

+ Customer Keyword Details

- Meta Data Information

*Issue Type
Qualification-Review-Issue

*Product Segment

- ☐ Product Hardware
- ☐ GPU Software
- ☐ Related Products
- ☐ PCIe Outcenter
- ☐ PCIe Driver
- ☐ Other
- ☐
- ☐

*Focus Area

- ☐ Project
- ☐ Client
- ☐ Server
- ☐ Network

- Attachments

Show details

Drag and Drop 1 or more files or Browse to Select

Submit Bug

Save as draft

Cancel

After submission, you can add comments and upload additional attachments through the Comments section.

Step 6: View Bug Status and Add Comments

After submitting, you can track your submission and provide additional information:

1. **View Bug Status:** Navigate to Bug > “View Bug Status” in the top menu. Search by Bug ID, synopsis, or other criteria. Click on the Bug ID to view full details.
2. **Add Comments:** From the bug detail page, scroll to the Comment Log section and click “Add Comment” to upload additional attachments or provide updates.



Note: Confidentiality

All submitted information is confidential and viewable only by the submitting partner and NVIDIA.

NVBug Notifications

Users receive system notifications (via email) whenever their NVBug submission is updated. These notifications include status changes, new comments, and resolution updates.

NVOnline Site Setup for Partners

Partners must have their NVOnline site properly configured to submit qualification bugs. The site must have “Customer Bug Forms Setup” enabled. The Qualification Review Bug Forms / Problem Types must also be activated.

Ensure the “Active” checkbox is selected. Contact your NVIDIA partner representative if your site is not configured correctly.

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